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Description

[POWER SUPPLY APPARATUS AND POWER SUPPLY CONTROL DEVICE]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] This invention relates to a power supply apparatus and a power supply control device, and particularly to a power supply apparatus and a power supply control device to reduce undershoot of source voltage when a power supply interrupt occurs.

[0003] Background of the Invention

[0004] Conventional integrated circuit power supply systems include, a DC/DC converter with a synchronous commutation type switching regulator. When a power supply incorporating a DC/DC converter experiences an interrupt, a synchronous commutation FET is commonly used to discharge an output capacitor on the low voltage side of the DC/DC converter.

[0005] However, this approach suffers from a rapid decrease in source voltage as the output capacitor discharges, which may result in voltage undershoot of the power supply. Japanese Published Unexamined Patent Application (PUPA) 10-295074 (pp. 3 and 6, Fig 2) discloses a method of preventing undershoot whereby a synchronous commutation FET coupled to the low voltage side of a DC/DC converter is turned off. At the onset of a power supply interrupt, an output capacitor is gradually discharged through a resistance connected between an output terminal of the source voltage and ground, which divides the voltage from the output terminal.

[0006] An aluminum or tantalum output capacitor is disclosed in Japanese PUPA 10-295074, which exhibits a dedicated polarity for each terminal and cannot be reverse biased without damaging the device. Therefore, discharging an output capacitor with an active synchronous commutation FET on the low voltage side of the DC/DC converter may result in a reverse bias of the output capacitor due to the voltage undershoot caused by the power supply interrupt, leading in turn to mechanical failure of the output capacitor. This is not an unusual occurrence since semiconductor devices connected to a power supply apparatus typi-

cally specify an allowable reverse voltage value. Accordingly, if reverse voltage with undershoot is applied to such a semiconductor device, malfunction or physical damage may result.

[0007] Conversely, if an output capacitor is gradually discharged while a synchronous commutation FET on the low voltage side of the DC/DC converter is turned off, the source voltage slowly decreases and a reverse voltage outside the specification of the semiconductor may be applied. In this instance, the probability of malfunction of the semiconductor is increased.

SUMMARY OF INVENTION

[0008] The purpose of this invention is to provide a power supply apparatus and a power supply control device, which can solve the above-described problems. According to a first aspect of the invention, a power supply apparatus adapted to supply a DC source voltage is provided that includes a source voltage supply unit to supply a source voltage to an output edge of the power supply apparatus. An output capacitor is coupled between the power supply output edge and ground and is discharged through a resistor coupled to a FET switch in the power supply control device. The discharge path is enabled in the event of a

power supply interrupt and disabled during continuous power supply operation.

Brief Description of Drawings

[0009] Fig. 1 illustrates the structure of the power supply apparatus 10 according to an embodiment of the invention;

[0010] Fig. 2 shows the source voltage waveform when halting power supply from the power supply apparatus 10 according to an embodiment of the invention:

[0011] Fig. 3 depicts a source voltage waveform when halting power supply from the power supply apparatus 10 according to another embodiment of the invention; and

[0012] Fig. 4 illustrates a control timing diagram from the start of supplying power to the termination of supplying power by the power supply apparatus 10 according to an embodiment of this invention.

Detailed Description

[0013] The present invention is directed to a power supply apparatus that reduces undershoot of source voltage and quickly discharges an output capacitor to mitigate the adverse effects of a power supply interrupt.

[0014] Fig. 1 shows a power supply 10 that supplies a DC source voltage Vout, and has a discharge path 132 to discharge

electrical charge accumulated in an output capacitor 115 through a discharge resistor 135 when a power supply interrupt occurs. During an interrupt, the power supply apparatus 10 turns on the discharge path 132 and discharges the output capacitor 115 according to an RC time constant controlled by the discharge resistor 135. The value of the resistor 135 may be set such that the degree of voltage undershoot is within a predefined value and the time until the source voltage decreases to zero, as measured from the interrupt of the supply, is within a specified time. The power supply apparatus 10 has a source voltage supply unit 100, an output capacitor 115, a output voltage coil 120 and a power supply control device 130.

[0015] The source voltage supply unit 100 supplies a DC source voltage to a power supply output 102 at the edge of the power supply apparatus 10. According to the invention, the source voltage supply unit 100 has a high voltage side switch 103 and a low voltage side switch 106.

[0016] A high voltage side switch 103 is provided between a voltage source, Vin and the power supply output edge. In Fig. 1, the high voltage side switch 103 is shown as a MOS type FET with the drain connected to the voltage source

Vin, and the source connected to the output voltage coil 120, the drain of the low voltage side switch 106 and the discharge path 132. If the source voltage, Vout supplied by the source voltage supply unit 100, is less than a predetermined voltage standard, the high voltage side switch 103 is turned on by the power supply control device 130. In this embodiment, the high voltage side switch 103 connects the voltage source Vin, which is higher than the source voltage Vout, to the power supply output edge 102 through the output voltage coil 120. The voltage source Vin is preferably higher than the standard voltage.

[0017] The low voltage side switch 106 is a FET, provided between ground and the power supply output edge 102. According to the present invention, the source and drain of the low voltage side switch 106 are connected to ground and the output voltage coil 120, respectively. If the source voltage, Vout is higher than the standard voltage, the low voltage side switch 106 is turned on by the power supply control device 130 to reduce the output voltage.

[0018] An output capacitor 115 is provided between the power supply output edge 102 and ground. One terminal of the output voltage coil 120 is connected to a node common to the source of the high voltage side switch 103 and the

drain of the low voltage side switch 106. The other terminal of the output voltage coil 120 is connected to the output capacitor 115 and the power supply output edge 102. The output voltage coil 120 supplies electric power to the output capacitor 115 and the power supply output edge 102.

[0019] The power supply control device 130 is a semiconductor device that controls the source voltage supply unit 100 when supplying a source voltage. In addition, the power supply control device 130 also controls discharge of the output capacitor 115 during a power supply interrupt. The power supply control device 130 has a discharge path 132, a source voltage controller 150, a timing controller 155 and an inverter logic element 160.

[0020] The discharge path 132 is connected between the source of the high voltage side switch 103 and the drain of the low voltage side switch 106 through a switching node terminal 170 of the power supply control device 130. The discharge path sinks electric charge accumulated in the output capacitor 115 to ground through the output voltage coil 120 and the switching node terminal 170 during a power supply interrupt. The discharge path 132 includes a discharge resistor 135, a discharge switch 140 and a

rectifier 145.

[0021] The discharge switch 140 is turned on to enable the discharge path 132 in the event of an interrupt to the source voltage supply. Conversely, if source voltage is being supplied, the discharge switch 140 is turned off to disable the discharge path 132. In this embodiment, the source and drain of the discharge switch 140 is connected to ground and one edge of the discharge resistor 135, respectively. A discharge rectifier 145 is provided to prevent current from flowing from the discharge path 132 to the power supply output edge 102. For example, when initializing the source voltage supply, the discharge rectifier 145 prevents switching current from flowing to the output voltage coil 120 and the power supply output edge 102 through the discharge path 132.

[0022] The source voltage controller 150 drives the gate of the high voltage side switch 103 included in the source voltage supply unit 100 and the gate of the low voltage side switch 106 through a high voltage side switch driving terminal 172 and a low voltage side switch driving terminal 174, respectively. These are the control inputs to the source voltage supply unit 100.

[0023] In addition, as in the case of the discharge path 132, the

source voltage controller 150 is connected between the source of the high voltage side switch 103 and the drain of the low voltage side switch 106 through the switching node terminal 170. When supplying source voltage, the source voltage controller 150 monitors source voltage input through the switching node terminal 170.

[0024] If source voltage is lower than the voltage required by the particular standard adopted, the source voltage controller 150 turns on the high voltage side switch 103 through the high voltage side switch driving terminal 172, and turns off the low voltage side switch 106 through the low voltage side switch driving terminal 174. Conversely, if the source voltage is higher than the standard voltage, the source voltage controller 150 turns on the low voltage side switch 106 through the low voltage side switch driving terminal 174, and turns off the high voltage side switch 103 through the high voltage side switch driving terminal 172. Accordingly, the source voltage controller 150 regulates the source voltage, Vout supplied to the power supply output edge 102 to equal the value of the standard voltage.

[0025] In addition, if supply of source voltage is interrupted, the source voltage controller 150 turns off the high voltage

side switch 103 and the low voltage side switch 106 through the high voltage side switch driving terminal 172 and the low voltage side switch driving terminal 174, respectively. In this regard, the source voltage controller 150 enables the discharge path 132 to discharge the output capacitor 115 in the event of an interruption of the source voltage supply.

[0026] Alternatively, if the power supply apparatus 10 or a device connected to the power supply apparatus 10 malfunctions or experiences an intermittent failure and supply of source voltage is halted, the source voltage controller 150 turns off the high voltage side switch 103 and turns on the low voltage side switch 106. This allows source voltage to decrease to 0 V more quickly compared to the case when the output capacitor 115 is dissipated through the discharge path 132.

[0027] The timing controller 155 controls operation timing of the source voltage controller 150 and the discharge path 132. An external signal controls the start and stop of the source voltage supply. More specifically, the timing controller 155 outputs a power signal that is asserted high when starting the supply of source voltage and asserted low if halting supply, to the source voltage controller 150.

When receiving the signal, the source voltage controller 150 starts or stops the supply of source voltage from the source voltage supply 100.

[0028] In addition, the timing controller 155 outputs a discharge path disable signal that is asserted low if discharging the output capacitor 115 and asserted high if not discharging the output capacitor 115 through the discharge path 132. The inverter logic element 160 inverts the logic value of the discharge path disable signal and inputs the results to the gate of the discharge switch 140. If the timing controller 155 asserts a discharge path disable signal, a logic "1" drives the gate of the discharge switch 140 to enable the discharge path 132. However, if the timing controller 155 asserts a high discharge path disable signal, the logic value "0" is input to the gate of the discharge switch 140 to turn off the discharge switch 140 and disconnect the discharge path 132.

[0029] The above-described power supply apparatus 10 turns off the high voltage side switch 103 and the low voltage side switch 106, and turns on the discharge switch 140 when the supply is interrupted, thereby enabling the output capacitor 115 to discharge through the discharge path 132. The amount of voltage undershoot is controlled by the

output capacitance and discharge resistance. Moreover, the time it takes the source voltage Vout to decrease to 0 volts upon the occurence of a power supply interrupt is similarly dependent on the RC time constant associated with the output capacitor 115 and discharge resistor 135. Ideally, this time constant is greater than or equal to the time it takes the source voltage, Vout to decrease to 0 volts. This enables the above-described power supply apparatus 10 to reduce voltage undershoot while rapidly discharging the output capacitor 115.

[0030] Fig. 2 shows an example of a source voltage waveform when the output voltage of the power supply apparatus 10 is interrupted. When a source voltage is supplied, the source voltage controller 150 controls the high voltage side switch 103 and the low voltage side switch 106 to allow a source voltage, which is supplied to the power supply output edge 102, to balance with a standard voltage. When a control signal to halt the supply of source voltage is received at time, t1, the timing controller 155 transmits a logic "0" power supply signal, which indicates the interrupt of the supply of source voltage to the source voltage controller 150, and transmits a logic "0" discharge path disable signal, which enables the discharge path 132.

When receiving the logic low discharge path disable signal, the source voltage controller 150 turns off the high voltage side switch 103 and the low voltage side switch 106, and the timing controller 155 turns on discharge switch 140 through the inverter element 160. This sequence enables electric charge accumulated in the output capacitor 115 to discharge through the output voltage coil 120, the switching node terminal 170, the discharge diode 145, the discharge resistor 135 and the discharge switch 140, so that source voltage at the power supply output edge 102 becomes 0 V at time t2.

[0031] The value of the discharge resistor 135 is determined according to the value of the output capacitor 115 so that the degree of undershoot is within a specified value. The duration of the undershoot component of the interrupted power supply signal is preferably within the time (t2 - t1) until the source voltage goes to 0 volts. Ideally, the time (t2 - t1) period during which the source voltage decreases to 0 volts is a few milliseconds. Therefore, if the value of the output capacitor 115 is a few hundred pF, a discharge resistor 135 value of about 1 ohm will produce a time constant in the range of 10 milliseconds or less.

[0032] According to a second embodiment of the invention, Fig.

3 shows a source voltage waveform steadily decreasing toward a threshold voltage at which point the power supply control apparatus sets the voltage supply to 0 volts. At time, t1, the timing controller 155 transmits a power supply signal "0" to the source voltage controller 150 indicating the source voltage is no longer being supplied. Next, the discharge path 132 is enabled. In response to the loss of power supply, the source voltage controller 150 turns off the high voltage side switch 103 and the low voltage side switch 106, and the timing controller 155 turns on the discharge switch 140 through the inverter element 160. Finally, the electric charge accumulated in the output capacitor 115 is discharged to ground through the output voltage coil 120, the switching node terminal 170, the discharge diode 145, the discharge resistor 135 and discharge switch 140.

[0033] At time, t2, the source voltage controller 150 turns on the low voltage side switch 106 after a predetermined time period following activation of the discharge path 132. At this point, the power supply output voltage is preferably within the range of a standard voltage and ground potential. When the power supply output decreases to Vt, the source voltage controller 150 turns on the low voltage

side switch 106 after the timing controller 155 enables the discharge path 132. Subsequent to t2, the source voltage controller 150 will regulate the discharge switch 140 as required to maintain Vout at 0 volts.

[0034] As the waveform in Fig. 3 approaches time, t3, the low voltage switch 106 provides a direct path between the output voltage node, Vout and ground, thereby driving the source voltage to 0 volts.

[0035] According to the second embodiment, when a power supply interrupt occurs, the discharge path 132 is conductive for a predetermined time and the source voltage is reduced to 0 V and the low voltage side switch 106 is turned on to allow source voltage to go to 0 volts without significant undershoot. Even if the low voltage side switch 106 is turned on to rapidly discharge the output capacitor 115, the source voltage, Vt at time, t2 is adjusted so that the value of undershoot of the source voltage is within a specified range. The power supply apparatus 10 maintains the value of undershoot within the specified range, and can tolerate a sudden loss of power supply voltage at a high speed.

[0036] Alternatively, in the above-described method corresponding to a second embodiment of the invention, after a pre-

determined time elapses following a loss of supply of source voltage and the discharge path 132 through the discharge switch 140 is conducting, the source voltage controller 150 may also turn on the low voltage side switch 106. In addition, as the source voltage approaches Vt, the source voltage controller 150 can measure source voltage through the switching node terminal 170, and then turn on the low voltage side switch 106.

[0037] Fig. 4 shows control timing from initialization of a power supply until the supply of power is terminated. At time, t1, the timing controller 155 receives a control signal, indicating an initial supply of a source voltage, from outside of the power supply control device 130. Once the On/Off control signal is asserted high, the timing controller 155 sets the discharge path disable signal to a logic "1" at t1 by opening the discharge switch 140. The timing controller 155 then asserts the power supply signal high at time, t2 and outputs the power supply signal to the source voltage controller 150 allowing the source voltage supply unit 100 to begin supplying a source voltage.

[0038] At time, t3, the timing controller 155 receives a control signal indicating the interruption of supply of source voltage, from outside of the power supply control device 130.

If the supply of source voltage is terminated after receiving the control signal, the timing controller 155 asserts the power supply signal to logic zero and outputs the power supply signal to the source voltage controller 150 at t3 to allow the source voltage supply unit 100 to terminate the supply of source voltage. The timing controller 155 then sets the discharge path disable signal to a logic "0" at time, t4, and closes the discharge switch 140 to discharge the output capacitor 115.

[0039] In the above-described power supply apparatus 10, the timing controller 155 manages operation timing of the source voltage controller 150 and the discharge path 132 so that the high voltage side switch 103 and the discharge switch 140 are not turned on at the same time. In the event the high voltage side switch 103 and the discharge switch 140 are turned on at the same time, the timing controller 155 can prevent an over-current condition by sinking the current flowing from the high voltage source, Vin to ground through the discharge path 132. Accordingly, the timing controller 155 can mitigate the risk of damage to internal circuits from sourcing a voltage in excess of the standard voltage utilized in the system.

[0040] While the invention has been described in detail, the fore-

going description is in all aspects illustrative and not restrictive. It is understood that numerous other modifications and variations can be devised without departing from the scope of the invention.

[0041] For example, the source voltage supply unit 100 in the embodiments may also be one of various power supply circuits, in which a voltage source is connected to the power supply output edge 102 through the output voltage coil 120 if source voltage is supplied and the voltage source is disconnected from the power supply output edge 102 if supply of source voltage is interrupted.

[0042] In addition, the switching node terminal 170 may also be LX (switching node) terminal of power source IC. Alternatively, the source voltage controller 150 and the discharge path 132 may also be connected to the power supply output terminal 102 through a different terminal of the power supply control device 130. Furthermore, the timing controller 155 and/or the discharge path 132 may also be provided external to the power supply control device 130.